REMARKS

Claims 1-23 are pending; claims 4, 5, 7, 12 and 23 have been amended in several particulars; and claims 24 and 25 are newly added in accordance with current Office policy, to alternatively define Applicant's invention and thereby assist the Examiner by facilitating the search and thus expediting the compacted prosecution.

The Examiner has objected to the drawings for failing to include reference "6B" and reference "2". Note that the Specification has been amended to change "6B" to --68-- as used in Fig. 3. Fig. 1 has been amended to show light source 68, and Fig. 3 has been amended to include reference numerals 1 and 2 as used in Fig. 1 (like elements in different figures of the drawings have the same reference label). Additionally, attached hereto are proposed drawing corrections submitted for the Examiner's approval. No new matter has been entered.

Claim1-17 and 23 were rejected under 35 U.S.C. §112, second paragraph based upon a number of deficiencies kindly noted by the Examiner. Accordingly the above amendment is believed to correct for those deficiencies not traversed below.

The Examiner's rejection of claim 1 states that claim 1 lacks sufficient structure to perform the function of *generating converted data by converting input data*. The specification states, page 8, lines 1-2, "transmitting unit 10 converts the print data to a series of lines of video data," as shown in Fig. 2. Therefore, the claim accurately sets forth the invention as disclosed. Accordingly, the rejection is deemed to be in error and should be withdrawn.

The Examiner also rejects claim 1 by stating that the claim recites two functions for a single means. Note that the specification states from page 7, line 18 through page 8, line 9, "data transmitting unit 10 receives printing data supplied from data output device 1 of a source such as a computer having a RIP (Raster Image Processor), via a bus line 2. Also, transmitting unit 10 converts the print data to a series of lines of video data in correspondence with a clock signal fed in via a line 52 and then, outputs the converted video data via line 12 in response to a horizontal synchronization signal exhibiting a predetermined time interval applied via a line 14," and claim 1 calls for *data transmitting means for generating converted data by converting input data to be printed into video data in accordance with a first clock signal, and for transmitting the converted data in response to a horizontal synchronization signal exhibiting a predetermined time interval.* Clearly claim 1 depicts the invention as disclosed. 35 U.S.C. §112, second paragraph states:

> "The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention."

Therefore, since claim 1 sets forth the invention as disclosed and the specification provides clear antecedent basis for the language set forth in claim 1, then the rejection is in error because claim 1 particularly points out and distinctly claims the subject matter which the Applicant regards as his invention. Additionally, there is no provision set forth in 35 U.S.C. §112, second paragraph which prohibits claim language for a single means for performing more than one function. *In re Kelley*, 134 USPQ 397 states:

> "We see no reason why a single structural element....which performs two separate functions, cannot support a claim reciting broadly these separate functions." See also *Palmer v. United States*, 163 USPQ 250

Further, 35 U.S.C. §112, sixth paragraph states:

> An element in a claim for a combination may be expressed as a means or step for performing a specified function without the recital of structure, material, or acts in support thereof, and such claim shall be construed to cover the corresponding structure, material, or acts described in the specification and equivalents thereof.

Note that §112, sixth paragraph, does not prohibit more than one function being specified for the claimed means, but instead denotes that the claimed means must have a function. In other words, one can not claim *means* without including a function for the *means*, because a *means* without a function makes no sense. Further, when using the term "means" without the recital of structure, material, or acts in support thereof, it would not be understood what the "means" should be construed to cover without recitation of the functions performed by the "means."

The Examiner further rejects claim 1 by stating that the claim recites a plurality of functions for the *control means*, and that the claim lack sufficient structure for performing the functions claimed. Note that the specification states on page 8, lines 5–12 states:

> "A printing control unit 20 controls a mechanism required for printing the video data with electrical signals and supplies beam data, used to switch the light generation of a light source element located in a beam scanning unit 30, to the light source element through a line 22 by obtaining the beam data via a line 12 from the video data received. Also, print control unit 20 receives beam detection signals generated by the light source element 68 for processing via a line 24 and then, supplies the horizontal synchronization signal to the line 14. In addition, the printing control unit 20 supplies a bias voltage control signal via a line 72 to a bias voltage generator 70."

Therefore, the claimed *print control means* has support in the specification in view of the printing control unit 20, and since the printing control unit 20 performs a plurality of functions, then the claimed *print control means* can also be accurately claimed to perform a plurality of functions. Additionally, the *print control means* does not require further structure to perform the functions

claimed since the printing control unit 20 is capable of performing the functions claimed. Therefore, the rejection is deemed to be in error and should be withdrawn.

The Examiner further yet rejects claim 1 and states that the claimed '[a] light source element' is not positively recited." What does the Examiner mean by "positively recited?" Why does the light source have to be positively recited? There is no provision in 35 U.S.C. §112, second paragraph which states all elements in a claim must be positively recited. §112, second paragraph, requires that the claim particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention. How does "not positively reciting a light source" cause the claim not to particularly point out and distinctly claim the subject matter which the applicant regards as his invention? Moreover, the "light source element" is not a component included within the definition of claim 1, but is an element in the nature of the workpiece. While claim 1 defines apparatus that contemplates operating upon a light beam provided by a source, that source itself is not a component part of the apparatus defined by claim 12. Accordingly, the rejection is deemed to be in error and should be withdrawn.

The rejection of claim 12 is not clear since there is no recitation in claim 12 for "in dependence upon a beam source" as suggested by the Examiner. Accordingly, the rejection is deemed to be in error and should be withdrawn.

Claims 1–23 were rejected under 35 U.S.C. §103, as rendered obvious and unpatentable, over Sasaki et al. in view of Nakajima. The applicant respectfully traverses this rejection for the following reason(s).

The Examiner's application of the art does not make any sense to the Applicant. It appears that the Examiner has repeated the claims language and merely inserted column and line numbers from the applied references to indicate where the limitations can be found. Note that the applied references include drawings wherein each element of the figures has a corresponding reference numeral. It would have been most helpful if the Examiner would have included these reference numerals along side the column and line numbers so that the Applicant could easily ascertain how the Examiner is attempting to apply the art.

The electrophotographic developing type reproduction apparatus of claim 1 calls for a *data transmitting means for generating converted data by converting input data to be printed into video data in accordance with a first clock signal, and for transmitting the converted data in response to a horizontal synchronization signal exhibiting a predetermined time interval*. The Examiner refers to Sasaki et al. col. 1, lines 54–58 and col. 3, lines 1–4, and Nakajima's abstract lines 13–16. Accordingly, we must assume that the Examiner has attempted to equate host 9 of Sasaki et al. with the *data transmitting means*, because there are no other means described in the cited columns and lines of Sasaki to indicate some other elements therein may comprise the data transmission means. Also, we must assume that the Examiner has attempted to equate the horizontal sync signal discussed in Nakajima with the *horizontal synchronization signal exhibiting a predetermined time interval*. However, we cannot presume how the Examiner is applying the foregoing teachings in order to provide a *prima facie* case of obviousness. The Examiner has not provide any information to suggest how the applied references are being combined. The Examiner has merely stated that "it would have been obvious....to incorporate the teachings of Nakajima in Sasaki et al. for the purpose of controlling the light signal of the electrophotographic device" without expressing how the references are to be combined. In other words, how is the horizontal sync signal of Nakajima

to be used in Sasaki et al.? Where is the *first clock signal* discussed in Sasaki et al.? If host 9 is the *data transmitting means*, where is there disclosure that host 9 converts input data to be printed into video data in accordance with a first clock signal? If host 9 is the *data transmitting means*, where is there disclosure that host 9 transmits the converted data in response to a some signal exhibiting a predetermined time interval such that one of ordinary skill in the art might equate this signal of a predetermined time interval with a horizontal sync signal? Note that the horizontal sync signal in Nakajima is output via an interface to an external apparatus but there is no disclosure in Nakajima to indicate what this external apparatus is or how it uses the horizontal sync signal. Therefore, it is not understood how the Examiner can even suggest that the horizontal sync signal output by Nakajima would find use in Sasaki et al. in view of the lack in both references of a teaching or suggestion for the use of such a horizontal sync signal. There must be some reason for making the modification. *In re Gordon,* 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984). Further, obviousness cannot be established by combining the teachings of the applied references absent some incentive to support the combination. *Carella v. Starlight Archery,* 804 F.2d 135, 231 USPQ 644 (Fed. Cir 1986). Note that claim 1 calls for the *printing control means* to generate the *horizontal synchronization signal*. Nakajima does not teach a print control means for generating a horizontal sync signal and Sasaki's *print control means*, *i.e.,* laser unit 14, does not generate a horizontal sync signal, and Nakajima does not disclose a print control means for generating a horizontal sync signal. Accordingly, since the Examiner has not established a *prima facie* case of obviousness with regard to the first and last clauses of claim 1, the rejection should be withdrawn. See also, the first and last clauses of claim 12 and the third and last clauses of claim 18.

The Examiner refers to col. 2, lines 34–39, for a teaching of a *chopping means*. Therefore, since col. 2, lines 34–39 are a discussion of "a video signal processor" then the video signal

processor 10 of Fig. 2 having the circuitry of Fig. 3 in Sasaki et al. is assumed to be the *chopping means* referred to by the Examiner. Claim 1 calls for the *chopping means for providing chopped data.... in accordance with a second clock signal,* and claim 2 calls for the *second clock signal* to have *a frequency greater than the first clock signal*. The Examiner refers to Sasaki et al. col. 4, lines 4–11 to apparently teach the second clock signal having a frequency greater than the first clock signal. A review of Sasaki et al. col. 4, lines 4–11, however, finds no teaching of the second clock signal having a frequency greater than the first clock signal, but instead there is a teaching of the second clock signal having "a frequency higher than that of the video data 1". Since the video data 1 is supposed to have been produced as a result of *converting input data to be printed into video data in accordance with a first clock signal,* as set forth in the first clause of claim 1, then the video data 1 of Sasaki et al. cannot be equated to be the *first clock signal*. Additionally, as noted earlier, Sasaki et al. makes no mention of *converting input data to be printed into video data in accordance with a first clock signal,* and the Examiner has not shown that such a first clock signal has been taught in Sasaki et al. Therefore, the rejection of claim 2 is deemed to be in error and should be withdrawn. See also claims 13 and 19.

Claim 3 calls for *a frequency of the second clock signal being an integer multiple of a frequency of the first clock signal,* and the Examiner has referred to Sasaki et al. col. 4, lines 19–22 as an apparent teaching of claim 3. A review of col. 4, lines 19–22 finds that Sasaki et al. teaches that four cycles of the clock signal correspond to one isolated dot in the video data 1. Accordingly, there is clearly no teaching that the clock signal CLK, *i.e.,* the *second clock signal*, is any multiple of another clock signal, much less *an integer multiple of a frequency of the first clock signal,* especially since Sasaki et al. makes no mention of *a first clock signal*. Therefore, the rejection of claim 3 is deemed to be in error and should be withdrawn. See also claim 14.

Claim 4 calls for *said chopping means comprising an AND gate having a first input port coupled to receive said converted data and a second input port coupled to received said second clock signal.* The Examiner refers to Fig. 3, elements 23, 30 and 32 and col. 5, lines 17–20 in Sasaki et al. for apparently teaching the claimed AND gate. Note, however, that in Fig. 3 of Sasaki et al. element 23 is a differentiating circuit, element 30 is a flip–flop and element 32 is a counter. Also, in col. 5, lines 17–20 of Sasaki et al. there is disclosure of an AND gate 33, however, AND gate 33 does not have an input port connected to receive *said second clock signal* nor does AND gate 33 have an input port coupled to receive *said converted data*.

The Examiner applies Nakajima for apparently teaching a *mode selecting means enabling a user to externally change a characteristic of said second clock signal*, as set forth in claim 5, and refers to the Abstract, lines 16–21 [15–20], in Nakajima, which state:

> "On the other hand, a receiver receives a stop request signal from the external apparatus. A controller controls the signal interface to stop the operations of the stepping motor and the signal interface, in response to the received stop request signal."

Accordingly, the foregoing quote from Nakajima's abstract, as applied by the Examiner, does not teach nor suggest controlling or changing the characteristics of a second clock signal. Further, Nakajima does not teach nor suggest use of a mode selecting means enabling a user to externally change a characteristic of a second clock signal. Additionally, the Examiner makes no effort to explain why or how Nakajima is supposed to be used in making any type of modification to Sasaki et al. Therefore, the rejection is deemed to be in error and should be withdrawn.

Claim 7 calls for *first means for generating a local clock signal; and second means for generating said second clock signal by dividing said local clock signal in dependence upon a*

dividing ratio component of said input data. The Examiner has referred to all of Fig. 3 in Sasaki et al. instead of to one or more specific elements of Fig. 3, in an erroneous attempt to suggest that Sasaki et al. teaches the features of claim 7. In Fig. 3 of Sasaki et al. there is shown an oscillator 31 for generating a clock signal CLK and a counter 32 for providing an more than one output to AND gate 33 based on counts of the clock signal CLK in response to the video data 1 input to the clear terminal of the counter 32. Accordingly, counter 32 does not divide the clock signal CLK to generate a second clock signal, and counter 32 does not depend upon a dividing ratio component of the input data (video data 1). Clock signal CLK is also provided to differentiating circuit 23, shift register 24 and shift register 26, none of which perform any division of the clock signal CLK. Therefore, the rejection is deemed to be in error and should be withdrawn. See claim 22, also.

Claim 8 calls for *means for generating a local clock signal; first means for generating said first clock signal by dividing said local clock signal; and second means for generating said second clock signal by dividing said local clock signal in dependence upon a dividing ratio component of said input data*, and is similar to claim 7 except that claim 8 includes the feature *first means for generating said first clock signal by dividing said local clock signal*. This time the Examiner has referred to col. 4, lines 23–38 in Sasaki et al., instead of Fig. 3. In col. 4, lines 23–38 Sasaki et al. discusses operations of the differentiating circuit 23, shift register 24 and shift register 26, none of which perform any division of the clock signal CLK. in Fig. 3 of Sasaki et al., and makes no mention of any means for dividing the clock signal CLK which is generated by oscillator 31. Therefore, the rejection is deemed to be in error and should be withdrawn. See claim 23, also.

The Examiner has referred to col. 4, lines 2–18 in Sasaki et al. for apparently teaching *said chopping means intermittently transmitting said serial video data during pulses of said second*

clock signal. Sasaki et al., col. 4, lines 2–18 do not make any mention of nor suggest *intermittently transmitting said serial video data during pulses of said second clock signal*. Accordingly, the rejection is deemed to be in error and should be withdrawn.

Claim 10 calls for *a component of said input data specifying a dividing ratio; and means for setting a frequency exhibited by said second clock signal in dependence upon said component*, and the Examiner erroneously suggests that these features of claim 10 are found in Sasaki et al. col. 4, lines 3–11. However, Sasaki et al., col. 4, lines 3–11 make no mention of any dividing ratio, makes no mention of the input data (video data 1) as having a component for specifying a dividing ratio, makes no mention of a second clock signal and makes no mention of any means for setting a frequency exhibited by the nonexistent second clock signal in dependence upon the nonexistent component. Accordingly, the rejection is deemed to be in error and should be withdrawn. See also claim 11, which also includes the feature of *said chopping means dividing said converted data into a series of pulses exhibiting a pulse frequency corresponding to said frequency exhibited by said second clock signal*, which the Examiner erroneously suggests is taught by Sasaki et al., col. 4, lines 11–23. Sasaki et al., col. 4, lines 11–23, discuss video data 1 input to differentiating circuit 23 to produce video data 1', and clock signal CLK produced by oscillator 31. Accordingly, there is no mention of any *second clock signal* nor any *frequency exhibited by said second clock signal*, in col. 4, lines 11–23, of Sasaki et al. Further, as can be seen from Sasaki et al., Fig. 5, neither video data 1' nor video data 2, both being some converted form of the input data (video data 1), comprise a series of pulses nor a series of pulses exhibiting a pulse frequency corresponding to a frequency exhibited by a nonexistent second clock signal. Accordingly, the rejection is deemed to be in error and should be withdrawn.

The Examiner's rejection on page 5, line 22 through page 6, line 11, of the Office action (Paper No. *unnumbered*), mailed 27 March 1995, appears to be directed toward the subject matter of claim 18. However, page 5, line 22 through page 6, line 11, of the Office action, is illogical. For example, the Examiner refers to Fig. 4A and col. 2, lines 6–21 of Sasaki et al. for teaching of *data bus means for providing input video data and for providing dividing ratio data; clock signal generating means for generating a first clock signal and for generating a second clock signal, said second clock signal exhibiting a characteristic depending upon said dividing ratio data;* and *data transmitting means for converting said input video data into serial video data in response to said first clock signal,* but col. 2, lines 6–21 in Sasaki et al. are a discussion of Sasaki et al.'s prior art figures 6A through 7E and have nothing to do with Fig. 4A in Sasaki et al. Likewise, col. 1, lines 12–33 of Sasaki et al. are a discussion of Japanese reference JP–A–61–234168 and therefore do no provide a teaching for the Sasaki et al. invention. Accordingly, the Examiner's rejection is not understood, is deemed to be in error, and should be withdrawn. Further, note that the arguments provided above are also deemed to be pertinent to the rejection of claim 18. For example, Sasaki et al., alone or in combination with Nakajima, fails to teach or suggest:

- data bus means....for providing dividing ratio data;
- clock signal generating means....for generating a second clock signal, said second clock signal exhibiting a characteristic depending upon said dividing ratio data;
- data transmitting means....for transmitting said serial video data in response to a horizontal synchronization signal;
- logic means for providing chopped video data in dependance upon said serial video data and said second clock signal; and
- printing control means generating said horizontal synchronizing signal in dependence upon said beam detection signal.

Therefore, the rejection is deemed to be in error and should be withdrawn.

It is noted herein, that the Examiner did not make mention of the features of claim 20 and thus did not attempt to positively apply §103 to claim 20. Accordingly, claim 20 should have been indicated to be allowable over the art of record.

The Examiner is hereby reminded of the provisions of 37 CFR §1.106(b) which states:

> In rejecting claims for want of novelty or for obviousness, the examiner must cite the best references at his command. When a reference is complex or shows or describes inventions other than that claimed by the applicant, the particular part relied on must be designated as nearly as practicable. The pertinence of each reference, if not apparent, must be clearly explained and each rejected claim specified.

Further, *Ex parte Levy*, 17 USPQ2d 1461, 1462 (1990) states:

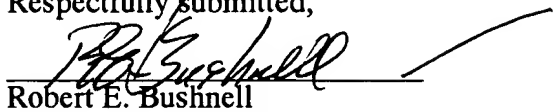
> "it is incumbent upon the examiner to identify wherein each and every facet of the claimed invention is disclosed in the applied reference."

Claims 24 and 25 are drafted after and include limitations found in claims 18 and 23 and 12+(13 through 16), respectively. Accordingly, claims 24 and 25 are deemed to be allowable over the art of record at least for the same reasons that claims 18 and 12 are allowable as discussed above.

The examiner is respectfully requested to reconsider the application, withdraw the objections and/or rejections and pass the application to issue in view of the above amendments and/or remarks.

A fee of $196.00 is incurred by the addition of two claims, which are independent claims, over the number of claims and independent claims previously paid for.

Respectfully submitted,



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